# 2500 MHz to 2900 MHz Rx Mixer with Integrated Fractional-N PLL and VCO

Preliminary Technical Data

# ADRF6604

## FEATURES

**Rx Mixer with Integrated Fractional-N PLL**
**RF Input Frequency Range: 1200 MHz to 3600 MHz**
**Internal LO Range: 2500 MHz to 2900 MHz**
**Input P1dB: +12dBm**
**Input IP3: +27dBm**
**IP3 Optimization via External Pin**
**SSB Noise Figure: 14dB**
**Voltage Conversion Gain: 6dB**
**Matched 200Ω IF Output Impedance**
**IF 3dB Bandwidth: 500MHz**
**Programmable via Three Wire SPI Interface**
**40 Pin 6mm x 6mm LFCSP Package**

## APPLICATIONS

**Cellular Base Stations**

| Part # | Internal LO Range | +/-3dB RF In Balun Range | +/-1dB RF In Balun Range |
|---|---|---|---|
| ADRF6601 | 750 MHz<br>1160 MHz | 300 MHz<br>2500 MHz | 450 MHz<br>1600 MHz |
| ADRF6602 | 1550 MHz<br>2150 MHz | 1000 MHz<br>3100 MHz | 1350 MHz<br>2750 MHz |
| ADRF6603 | 2100 MHz<br>2600 MHz | 1100 MHz<br>3200 MHz | 1450 MHz<br>2850 MHz |
| ADRF6604 | 2500 MHz<br>2900 MHz | 1200 MHz<br>3600 MHz | 1600 MHz<br>3200 MHz |

## GENERAL DESCRIPTION

The ADRF6604 is a high dynamic range active mixer with integrated PLL and VCO. The PLL/Synthesizer uses a Fractional-N PLL to generate a $F_{LO}$ input to the mixer. The reference input can be divided or multiplied then applied to the PLL phase detector. The PLL can support input reference frequencies between 12MHz and 160MHz. The phase detector output controls a charge pump whose output is integrated in an off-chip loop-filter. The loop filter output is then applied to an integrated VCO. The VCO output at $2*F_{LO}$ is then applied to a LO divider as well as to a programmable PLL divider.

The programmable divider is controlled by a sigma-delta modulator (SDM). The modulus of the SDM can be programmed between 2 and 2047.

The active mixer converts the single-ended 50Ω RF input to a 200 Ω differential IF output. The IF output can operate up to 500 MHz.

The ADRF6604 is fabricated using an advanced silicon-germanium BiCMOS process. It is available in a 40-lead, exposed-paddle, Pb-free, 6mm x 6mm LFCSP package. Performance is specified over a –40°C to +85°C temperature range.

## FUNCTIONAL BLOCK DIAGRAM

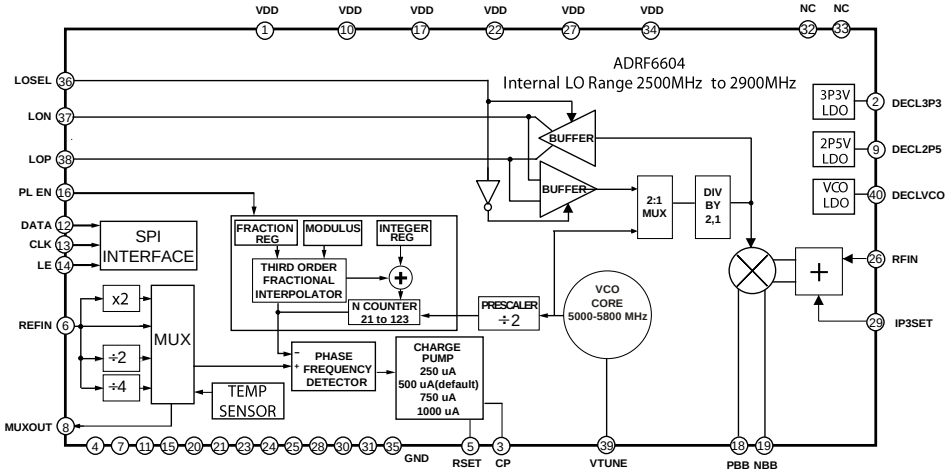


*Figure 1. ADRF6604 Block Diagram*



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## REVISION HISTORY

**6/09 Rev B, created from Rev A using ADI Template**
**6/09 Rev C, updated LO In, RF out, and VCO frequencies, updated register information, updated block diagrams. Added spec for RF Input Frequency range and for LO to IF leakage.**
**8/09 Rev D, updated to keep consistent with rev 0 Outline, updated registers per latest information, added main body text**

# SPECIFICATIONS

$V_S$ = 5V; Ambient Temperature ($T_A$) = 25°C; $F_{REF}$ = 76.8MHz; $F_{IF}$ = 153MHz; $F_{RF}$ = 2600MHz unless otherwise noted

**Table 1.**

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Frequency Range | | 2500 | | 2900 | |
| RF Input Frequency Range | +/-3dB | 300 | | 2500 | |
| RF INPUT @2400MHz | | | | | |
| Input return loss | Relative to 50Ω (can be improved with external match) | | 12 | | dB |
| Input P1dB | | | 12 | | dBm |
| Second Order Intercept (IIP2) | -6dBm Each Tone | | 55 | | dBm |
| Third Order Intercept (IIP3) | -6dBm Each Tone | | 27 | | dBm |
| Noise Figure | Single Side Band | | 14 | | dB |
| | With a -4dBm Interferer 5MHz Away | | TBD | | dB |
| IF/2 Spurious (2x2 IMD product) | IF = 150MHz | | TBD | | dBc |
| LO to RF Leakage | At 1x LO Frequency, 50Ω Termination at the RF Port | | -35 | | dBm |
| RF INPUT @2600MHz | | | | | |
| Input return loss | Relative to 50Ω (can be improved with external match) | | 12 | | dB |
| Input P1dB | | | 12 | | dBm |
| Second Order Intercept (IIP2) | -6dBm Each Tone | | 55 | | dBm |
| Third Order Intercept (IIP3) | -6dBm Each Tone | | 27 | | dBm |
| Single Side Band Noise Figure | | | 14 | | dB |
| | With a -4dBm Interferer 5MHz Away | | TBD | | dB |
| IF/2 Spurious (2x2 IMD product) | IF = 150MHz | | TBD | | dBc |
| LO to RF Leakage | At 1x LO Frequency, 50Ω Termination at the RF Port | | -35 | | dBm |
| IF OUTPUT | | | | | |
| Voltage Conversion Gain | 200Ω Load | | TBD | | dB |
| IF Bandwidth | Small Signal 3dB Bandwidth | | 500 | | MHz |
| | 1V p-p Signal 3dB Bandwidth | | TBD | | MHz |
| Output Common Mode Voltage | External Pull-up Balun or Inductors Required | | 5 | | V |
| Group Delay Flatness | Any 5MHZ/50MHz | | TBD | | ns p-p |
| Gain Flatness | Over RF Frequency Range, any 5MHZ/50MHz | | 0.2/1.0 | | dB |
| Gain Flatness | Over Frequency Range, any 5MHZ/50MHz | | 0.2/1.0 | | dB |
| Gain Variation | Over Full Temp Range | | 1.0 | | dB |
| Output Swing | Differential 200Ω Load | | 2 | | V p-p |
| Output Return Loss | Relative to 200Ω | | TBD | | dB |
| LO to IF Leakage | | | TBD | | dB |
| LO INPUT/OUTPUT | LOP, LON | | | | |
| Frequency Range | Externally Applied LO Input | 250 | | 6000 | MHz |
| Output Level (LO as Output) | 1x LO into a 50Ω Load, LO Output Buffer Enabled | | TBD | | dBm |
| Input Level (LO as Input) | Externally Applied 1x LO, Internal PLL Disabled | | 0 | | dBm |
| Input Impedance | | | 50 | | 50Ω |

# SPECIFICATIONS

$V_S$ = 5V; Ambient Temperature ($T_A$) = 25ºC; $F_{REF}$ = 76.8MHz; $F_{IF}$ = 153MHz; $F_{RF}$ = 2600MHz unless otherwise noted

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SYNTHESIZER SPECIFICATIONS | Synthesizer Specifications Referenced to 1x LO | | | | |
| Frequency Range | Internally Generated LO | 2500 | | 2900 | MHz |
| Figure of Merit | | | TBD | | dBc/Hz |
| Spurs | | | | | |
| Fractional Spurs | Offset from Integer LO SDM Modulus = 1536, $F_{PFD}$ = 38.4 MHz) | | | | |
| | 100kHz | | -54 | | dBc |
| | 200kHz | | -60 | | dBc |
| | 400kHz | | -66 | | dBc |
| | 800kHz | | -70 | | dBc |
| Reference Spurs | $F_{REF}$ = 76.8MHz | | | | |
| | $F_{REF}$/2 | | -80 | | dBc |
| | $F_{REF}$ | | -80 | | dBc |
| | >$F_{REF}$ | | TBD | | dBc |
| PHASE NOISE | Frequency = 2500 to 2900 MHz, PFD Frequency= 30.72 MHz or 38.4 MHz | | | | |
| | @ 1 kHz to 10 kHz offset | | -85 | | dBc/Hz |
| | @ 100 kHz offset | | -103 | | dBc/Hz |
| | @ 500 kHz offset | | -123 | | dBc/Hz |
| | @ 1 MHz offset | | -130 | | dBc/Hz |
| | @ 5 MHz offset | | -143 | | dBc/Hz |
| | @ 10 MHz offset | | -150 | | dBc/Hz |
| | @ 20 MHz offset | | -156 | | dBc/Hz |
| Integrated Phase Noise | 1 KHz to 10 MHz integration bandwidth | | 0.75 | | °rms |
| Frequency Settling | | | 1.0 | | ms |
| Phase Detector Frequency | Min/Max | | 24/40 | | MHz |
| REFERENCE CHARACTERISTICS | REFIN, REFOUT | | | | |
| REFIN Input Frequency | Min/Max | | 12/160 | | MHz |
| REFIN Input Capacitance | | | | 4 | pF |
| REFIN Input Current | | | | ±100 | µA |
| REFOUT Output Swing | Load ≤ 5 pF (REFIN = 76.8 MHz), Load ≤ 10 pF (REFIN = 38.4 MHz) | 0.25 | | 2.7 | V |
| REFOUT Duty Cycle | | 45 | | 55 | % |
| CHARGE PUMP | | | | | |
| Pump Current | Programmable to 250uA, 500uA, 750uA, 1000uA | | 500 | | uA |
| Output Compliance Range | | 1 | | 2.8 | Volts |

# SPECIFICATIONS

$V_S$ = 5V; Ambient Temperature ($T_A$) = 25°C; $F_{REF}$ = 76.8MHz; $F_{IF}$ = 153MHz; $F_{RF}$ = 2600MHz unless otherwise noted

| Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| LOGIC INPUTS | CLK, DATA, LE | | | | |
| $V_{INH}$, Input High Voltage | | 1.4 | | 3.3 | V |
| $V_{INL}$, Input Low Voltage | | 0 | | 0.7 | V |
| $I_{INH}/I_{INL}$, Input Current | | | ±TBD | | µA |
| $C_{IN}$, Input Capacitance | | | TBD | | pF |
| POWER SUPPLIES | Pins VCC, VCCbb, VCCrf | | | | |
| Voltage Range | VCC, VCCbb, VCCrf | 4.75 | 5 | 5.25 | V |
| Supply Current | PLL only | | 85 | | mA |
| | Normal Mode (Internal PLL Disabled) | | 150 | | mA |
| | Calibration Mode (Internal PLL Enabled) | | 240 | | mA |
| | Power Down Mode | | TBD | | uA |

# TIMING CHARACTERISTICS[1]

$V_{DD}$ = 5 V ± 5%;

**Table 2.**

| Parameter | Limit | Unit | Test Conditions/Comments |
|---|---|---|---|
| $t_1$ | 20 | ns min | LE Setup Time |
| $t_2$ | 10 | ns min | DATA to CLOCK Setup Time |
| $t_3$ | 10 | ns min | DATA to CLOCK Hold Time |
| $t_4$ | 25 | ns min | CLOCK High Duration |
| $t_5$ | 25 | ns min | CLOCK Low Duration |
| $t_6$ | 10 | ns min | CLOCK to LE Setup Time |
| $t_7$ | 20 | ns min | LE Pulse Width |

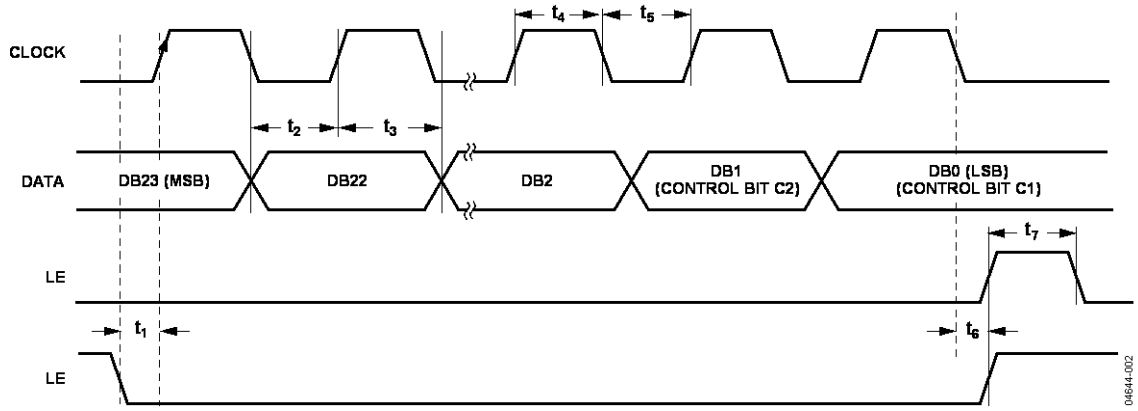


*Figure 2. Timing Diagram*

# ABSOLUTE MAXIMUM RATINGS

**Table 3. ADRF6604 Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Supply Voltage VCC, VCCbb, VCCrf | -0.5 to 6 V |
| Digital I/O CLK, DATA, LE | -0.3 to 3.3 V |
| IHI, ILO, QHI, QLO. RFIP | TBD V |
| $\theta_{JA}$ (Exposed Paddle Soldered Down) | TBD °C/W |
| Maximum Junction Temperature | 125°C |
| Operating Temperature Range | -40°C to +85°C |
| Storage Temperature Range | –65°C to +150°C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 40 Lead LFCSP_VQ | TBD | TBD | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# FUNCTIONAL BLOCK DIAGRAM

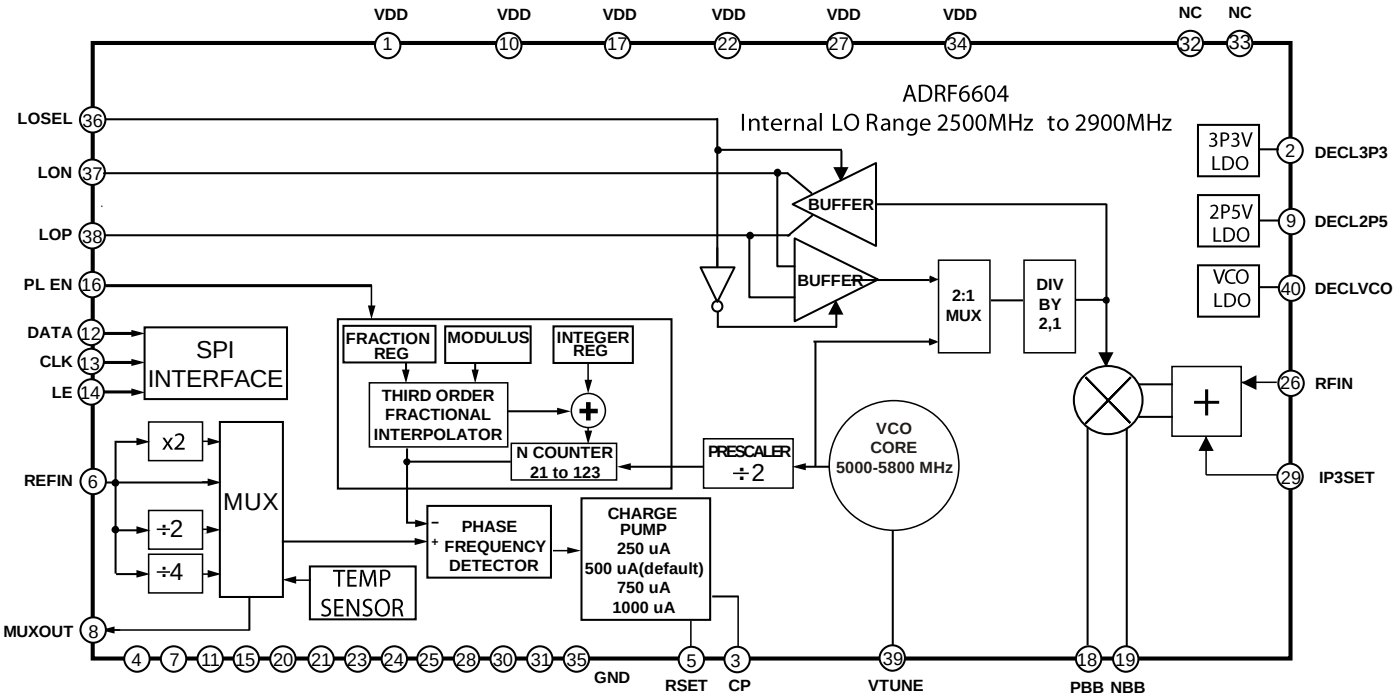


*Figure 3. ADRF6604 Functional Block Diagram*

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**Table 5. ADRF6604 Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| **Pin Nr.** | **Mnemonic** | **Description** |
| 1,10,17, 22,27,34 | VCC, VCClo, VCCbb, VCCrf | **Power Supply**: Power supply voltage range is 4.75 V to 5.25 V. Each pin should be decoupled with a 100 pf and 0.1uF capacitors located close to the pin. |
| 2 | DECL3P3 | **Decoupling Nodes for 3.3V LDO**: Connect a 0.1uF capacitor between this pin and ground. |
| 3 | CP | **Charge Pump**: Chargepump Output Pin. Connect to $V_{TUNE}$ through loop filter |
| 4,7,11,15, 20,21,23, 24,25,28, 30,31,35 | GND | **Ground**: Connect these pins to a low impedance ground plane. |
| 5 | $R_{SET}$ | **Charge Pump Current**: The nominal charge pump current can be set to either 250 uA, 500 uA, 750 uA or 1 mA using DB10 and DB11 of Register 4 and by setting DB18 to 0 (Internal Reference Current). In this mode, no external $R_{SET}$ is required. If DB18 is set to 1, the four nominal charge pump currents ($I_{NOMINAL}$) can be externally tweaked according to the equation. $$R_{SET} = \left[\frac{217.4 \times I_{CP}}{I_{NOMINAL}}\right] - 37.8[\Omega]$$ |
| 6 | $REF_{IN}$ | **Reference Input**: Nominal input level is 1Vpp. Input range is 12 MHz to 160 MHz. |
| 8 | MUXOUT | **Multiplexer Output**: This output can be programmed to provide the Reference Output signal or the Lock Detect signal. The output is selected by programming the appropriate register. |
| 9 | DECL2P5 | **Decoupling Nodes for 2.5V LDO**: Connect a 0.1uF capacitor between this pin and ground. |
| 12 | DATA | **Serial Data Input**: The serial data input is loaded MSB first with the three LSBs being the control bits. |
| 13 | CLK | **Serial Clock Input**: This serial clock input is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. Maximum clock frequency is 20 MHz. |
| 14 | LE | **Load Enable**: When the LE input pin goes high, the data stored in the shift registers is loaded into one of the six registers, the relevant latch being selected by the first three control bits of the 24-bit word. |
| 16 | PLL_EN | **PLL Enable**: Switch between Internal PLL and External LO Input. When this pin is logic high the mixer LO is automatically switched to the internal PLL and the internal PLL is powered up. When this pin is logic low the internal PLL is powered down and the external LO input is routed to the mixer LO inputs. The SPI may alternativly be used to switch modes. |
| 18,19 | PBB, NBB | **Mixer IF Outputs**: Should be pulled to VCC with RF Chokes |
| 26 | $RF_{IN}$ | **RF Input:** Single-ended, 50 Ω RF Input. |
| 29 | IP3Set | **IP3Set**: Connect resistor to VCC to adjust IP3 : Nominally leave open |
| 33,32 | NC | No Connection |
| 36 | LODRV_EN | **LO Driver Enable**: Together with Pin 16 (PLL_EN), this digital input pin determines whether the LOP and LON pins operate as inputs or outputs, as shown in the next section. LOP and LON become inputs if the PLL_EN pin is low or if the PLL_EN pin is set high with PLEN bit (DB6) Register 5 set to low. LOP and LON become outputs if either the LODRV_EN pin or LDRV bit (DB3) of Register 5 is set high while the PLL_EN pin is set high. External LO drive frequency must be 1xLO.<br>This pin should not be left floating. |
| 37,38 | LON, LOP | **Local Oscillator Input/Output**: The internally generated 1XLO is available on these pins.<br>When internal LO generation is disabled, an external 1XLO can be applied to these pins. |
| 39 | VTUNE | **VCO Control Voltage Input**: This pin is driven by the output of the loop filter. Nominal input voltage range on this pin is 1.5 V to 2.5 V |
| 40 | DECLVCO | **Decoupling Nodes for VCO LDO**: Connect a 100 pF and a 10uF capacitor between this pin and ground. |
| | EP | Exposed Paddle: The exposed paddle should be soldered to a low impedance ground plane. |

# TYPICAL PERFORMANCE CHARACTERISTICS

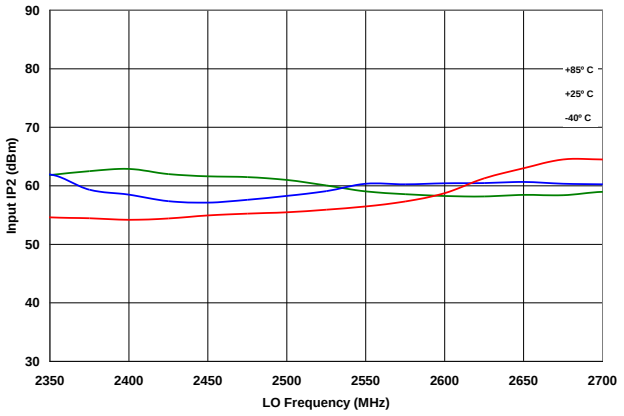


*Figure 4. ADRF6604 IIP2 vs. LO Frequency, Internally Generated LO, RF In = -10dBm, IF Out = 139/140MHz*

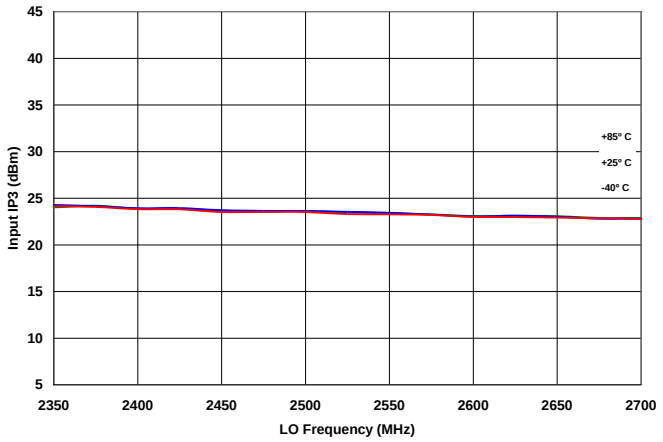


*Figure 5. ADRF6604 IIP3 vs. LO Frequency, Internally Generated LO, RF In = -10dBm, IF Out = 139/140MHz, IP3SET pin open, CAPDAC not optimized*

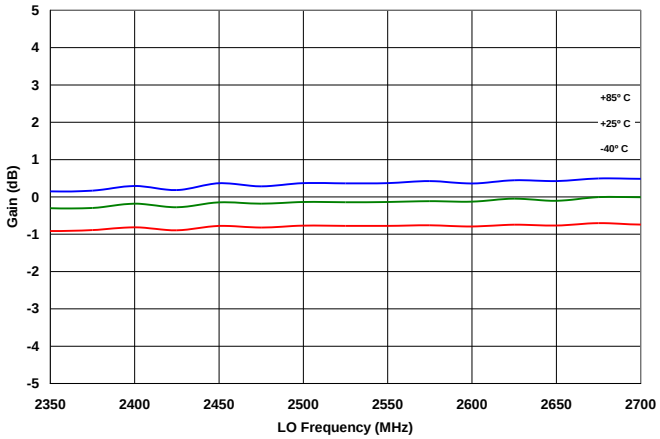


*Figure 6. ADRF6604 Gain vs. LO Frequency, Internally Generated LO, RF In = -10dBm, IF Out = 139/140MHz*

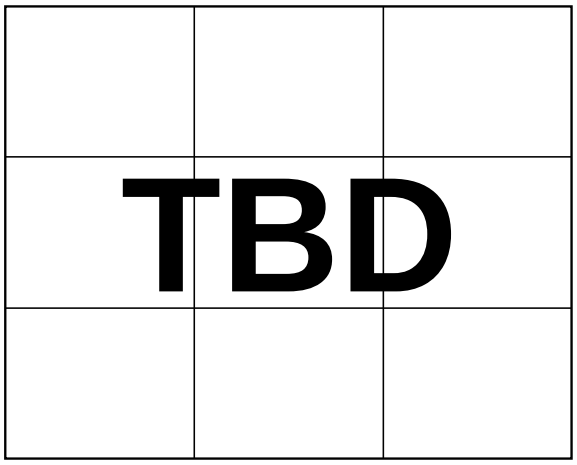


*Figure 7. . ADRF6604 Integrated and Spot Phase Noise vs. LO Frequency, Internally Generated LO, RF In = -10dBm, IF Out = 139/140MHz*

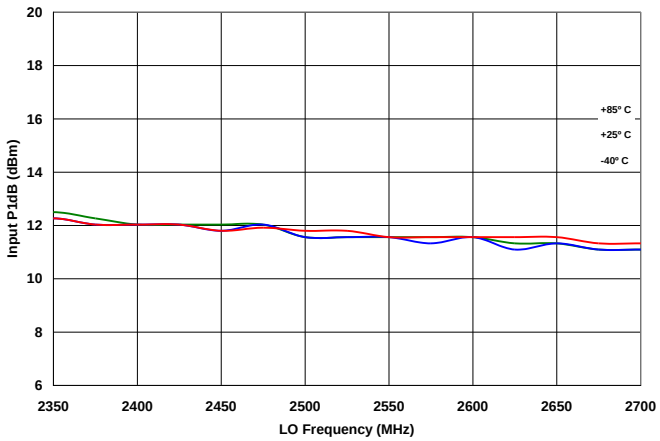


*Figure 8. ADRF6604 P1dB vs. LO Frequency, Internally Generated LO, RF In = -10dBm, IF Out = 139/140MHz*

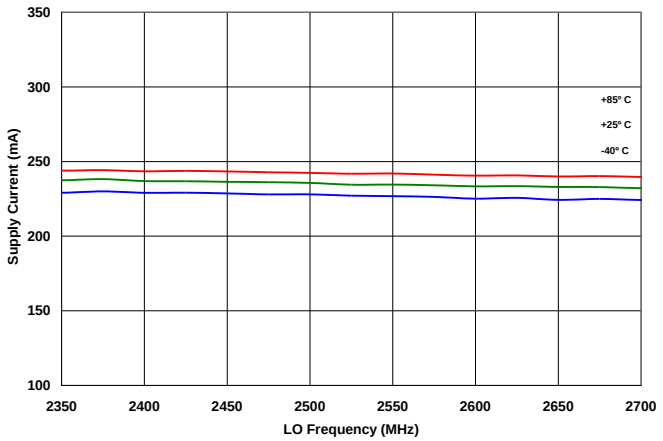


*Figure 9. . ADRF6604 Supply Current vs. LO Frequency, Internally Generated LO, RF In = -10dBm, IF Out = 139/140MHz*

# REGISTER STRUCTURE

*Table 6. Register Maps for ADRF6601. The three LSBs determine which register is programmed*

**REGISTER 0 – INTEGER DIVIDE CONTROL (default: 0x0001C0)**

| | | | | | | | | | | | | | DIVIDE MODE | INTEGER DIVIDE RATIO | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | DM | ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | C3(0) | C2(0) | C1(0) |

| DM | DIVIDE MODE |
|---|---|
| 0 | FRACTIONAL (DEFAULT) |
| 1 | INTEGER |

| ID6 | ID5 | ID4 | ID3 | ID2 | ID1 | ID0 | Divide Ratio |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 21 (Integer mode only) |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 22 (Integer mode only) |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 23 (Integer mode only) |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 24 |
| - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 56 (default) |
| - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 119 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 120 (Integer mode only) |
| 1 | 1 | 1 | 1 | 0 | 0 | 1 | 121 (Integer mode only) |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 122 (Integer mode only) |
| 1 | 1 | 1 | 1 | 0 | 1 | 1 | 123 (Integer mode only) |

**REGISTER 1 – MODULUS DIVIDE CONTROL (default: 0x003001)**

| | | | | | | | | | | MODULUS DIVIDE RATIO | | | | | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | MD10 | MD9 | MD8 | MD7 | MD6 | MD5 | MD4 | MD3 | MD2 | MD1 | MD0 | C3(0) | C2(0) | C1(1) |

| MD10 | MD9 | MD8 | MD7 | MD6 | MD5 | MD4 | MD3 | MD2 | MD1 | MD0 | Modulus |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1536 (default) |
| - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 2047 |

### REGISTER 2 – FRACTIONAL DIVIDE CONTROL (default: 0x001802)

| | | | | | | | | | | FRACTIONAL DIVIDE RATIO | | | | | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 | C3(0) | C2(1) | C1(0) |

| FD10 | FD9 | FD8 | FD7 | FD6 | FD5 | FD4 | FD3 | FD2 | FD1 | FD0 | Fractional Value |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 768 (default) |
| - | - | - | - | - | - | - | - | - | - | - | - |
| - | - | - | - | - | - | - | - | - | - | - | - |
| Fractional Value must be less than Modulus | | | | | | | | | | | <MDR |

### REGISTER 3 – SIGMA DELTA MODULATOR DITHER CONTROL (default: 0x10000B)

| | Dither Magnitude | | Dither Enable | Dither Restart Value | | | | | | | | | | | | | | | | | Control Bits | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | DITH1 | DITH0 | DEN | DV16 | DV15 | DV14 | DV13 | DV12 | DV11 | DV10 | DV9 | DV8 | DV7 | DV6 | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 | C3(0) | C2(1) | C1(1) |

| DITH1 | DITH0 | Dither Magnitude |
|---|---|---|
| 0 | 0 | 15 (default) |
| 0 | 1 | 7 |
| 1 | 0 | 3 |
| 1 | 1 | 1 (recommended) |

| DEN | Dither Enable |
|---|---|
| 0 | Disable (recommended) |
| 1 | Enable (default) |

| DV16 | DV15 | DV14 | DV13 | DV12 | DV11 | DV10 | DV9 | DV8 | DV7 | DV6 | DV5 | DV4 | DV3 | DV2 | DV1 | DV0 | Dither Restart Value |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0x00001 (default) |
| ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' |
| ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' | ' |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0x1FFFF |

## REGISTER 4 – CHARGE PUMP, PFD AND REFERENCE PATH CONTROL (default: 0x0AA7E4)

| REF OUPUT MUX SELECT | | | INPUT REF PATH | | CP MUX | CPB DIR | CP BLEED CURRENT | | | | | CP PUMP CURRENT | | CP SRC | CP CONTROL | | PFD EDGE | | PFD ANTI BACKLASH DELAY | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| RMS2 | RMS1 | RMS0 | RS1 | RS0 | CPM | CPBD | CPB4 | CPB3 | CPB2 | CPB1 | CPB0 | CPP1 | CPP0 | CPS | CPCT1 | CPCT0 | PE1 | PE0 | PAB1 | PAB0 | C3(1) | C2(0) | C1(0) |

| PAB0 | PAB1 | PFD ANTI BACKLASH DELAY |
|---|---|---|
| 0 | 0 | 0ns (DEFAULT) |
| 0 | 1 | 0.5ns |
| 1 | 0 | 0.75ns |
| 1 | 1 | 0.9ns |

| PE0 | REFERENCE PATH EDGE SENSITIVITY |
|---|---|
| 0 | FALLING EDGE |
| 1 | RISING EDGE (DEFAULT) |

| PE1 | DIVIDER PATH EDGE SENSITIVITY |
|---|---|
| 0 | FALLING EDGE |
| 1 | RISING EDGE (DEFAULT) |

| CPC1 | CPC0 | CHARGE PUMP CONTROL |
|---|---|---|
| 0 | 0 | BOTH ON |
| 0 | 1 | PUMP DOWN |
| 1 | 0 | PUMP UP |
| 1 | 1 | TRISTATE (DEFAULT) |

| CPS | CHARGE PUMP CONTROL SOURCE |
|---|---|
| 0 | CONTROL BASED ON STATE OF DB7/DB8 (CP CONTROL) |
| 1 | CONTROL FROM PFD (DEFAULT) |

| CPP1 | CPP0 | CHARGE PUMP CURRENT MULTIPLIER |
|---|---|---|
| 0 | 0 | 1x |
| 0 | 1 | 2x (DEFAULT) |
| 1 | 0 | 3x |
| 1 | 1 | 4x |

| CPB4 | CPB3 | CPB2 | CPB1 | CPB0 | PFD PHASE OFFSET MULTIPLIER |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | $0x22.5°/I_{CPMULT}$ |
| 0 | 0 | 0 | 0 | 1 | $1x22.5°/I_{CPMULT}$ |
| 0 | 0 | 1 | 0 | 0 | $4x22.5°/I_{CPMULT}$ (RECOMMENDED) |
| 0 | 1 | 0 | 1 | 0 | $10x22.5°/I_{CPMULT}$ (DEFAULT) |
| 1 | 0 | 0 | 0 | 0 | $16x22.5°/I_{CPMULT}$ |
| 1 | 1 | 1 | 1 | 1 | $31x22.5°/I_{CPMULT}$ |

| CPBD | PFD PHASE OFFSET POLARITY |
|---|---|
| 0 | NEGATIVE |
| 1 | POSITIVE (DEFAULT) |

| CPM | CHARGE PUMP CURRENT REFERENCE SOURCE |
|---|---|
| 0 | INTERNAL (DEFAULT) |
| 1 | EXTERNAL |

| RS0 | RS1 | INPUT REFERENCE PATH SOURCE |
|---|---|---|
| 0 | 0 | 2X REFIN |
| 0 | 1 | REFIN (DEFAULT) |
| 1 | 0 | 0.5X REFIN |
| 1 | 1 | 0.25X REFIN |

| RMS2 | RMS1 | RMS0 | OUTPUT MUX SOURCE |
|---|---|---|---|
| 0 | 0 | 0 | LOCK DETECT (DEFAULT) |
| 0 | 0 | 1 | VPTAT |
| 0 | 1 | 0 | REFIN (BUFFERED) |
| 0 | 1 | 1 | 0.5X REFIN (BUFFERED) |
| 1 | 0 | 0 | 2X REFIN (BUFFERED) |
| 1 | 0 | 1 | TRISTATE |
| 1 | 1 | 0 | 0.25X REFIN (BUFFERED) |
| 1 | 1 | 1 | DGND |

## REGISTER 5 – LO PATH AND MODULATOR CONTROL (default: 0x0000E5)

| | | | | | | | | | | | | CAP DAC | | | | LO DIV2 | PLL EN | LO DIV1 | LO EXT | LO DRV | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | | | | | | | | | | | CD3 | CD2 | CD1 | CD0 | LDV2 | PLEN | LDV1 | LXL | LDRV | C3(1) | C2(0) | C1(1) |

| CD3 | CD2 | CD1 | CD0 | CAPACITOR DAC CONTROL FOR IIP3 OPTIMIZATION |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | MIN |
| 1 | 1 | 1 | 1 | MAX |

| LDRV | LO OUTPUT DRIVER ENABLE |
|---|---|
| 0 | DRIVER OFF (DEFAULT) |
| 1 | DRIVER ON |

| LDV2 | ADDITIONAL DIVIDE-BY-2 IN LO CHAIN FOR ADRF6601, NOT AN OPTION FOR ADRF6602, 03,04 |
|---|---|
| 0 | DIVIDE BY 1 |
| 1 | DIVIDE BY 2 (DEFAULT) |

| LXL | EXTERNAL LO DRIVE ENABLE (PINS 37,38) |
|---|---|
| 0 | INTERNAL LO OUTPUT (DEFAULT) |
| 1 | EXTERNAL LO INPUT |

| LDV1 | DIVIDE BY 2 IN LO CHAIN ENABLE |
|---|---|
| 0 | DIVIDE BY 1 |
| 1 | DIVIDE BY 2 (DEFAULT) |

| PLEN | PLL ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE (DEFAULT) |

## REGISTER 6 VCO CONTROL AND ENABLES (default: 0x1E2106)

| | | | CHARGE PUMP ENABLE | 3.3V LDO ENABLE | VCO LDO ENABLE | VCO ENABLE | VCO SWITCH | VCO CALIBRATION | | | | | | VCO SW BS CTRL | VCO BAND SELECT FROM SPI | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| | | | CPEN | L3EN | LVEN | VCO EN | VCO SW | VC5 | VC4 | VC3 | VC2 | VC1 | VC0 | VBSRC | VBS5 | VBS4 | VBS3 | VBS2 | VBS1 | VBS0 | C3(1) | C2(1) | C1(0) |

| VC[5:0] | VCO AMPLITUDE |
|---|---|
| 0x00 | 0 |
| .... | .... |
| 0x18 | 24 (DEFAULT) |
| .... | .... |
| 0x2B | 63 (RECOMMENDED) |

| VBS[5:0] | VCO BAND SELECT FROM SPI |
|---|---|
| 0x00<br>0x01<br>....<br>0x1F | DEFAULT 0x10 |

| CPEN | CHARGE PUMP ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE(DEFAULT) |

| L3EN | 3.3V LDO ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE(DEFAULT) |

| VCO SW | VCO SWITCH CONTROL FROM SPI |
|---|---|
| 0 | REGULAR (DEFAULT) |
| 1 | BAND CAL |

| VBSRC | VCO BAND CAL & SW SOURCE CONTROL |
|---|---|
| 0 | BAND CAL (DEFAULT) |
| 1 | SPI |

| LV EN | VCO LDO ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE(DEFAULT) |

| VCO EN | VCO ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE(DEFAULT) |

## REGISTER 7 SPARE REGISTERS (default: 0x000007)

| | XVCO | MOD B_EN | | | | | | | | | | | | | | | | | | | CONTROL BITS | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| 0 | XVCO | MBE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | C3(1) | C2(1) | C1(1) |

| SPR18 | MODULATOR BIAS ENABLE |
|---|---|
| 0 | DISABLE |
| 1 | ENABLE (DEFAULT) |

| SPR19 | EXTERNAL VCO |
|---|---|
| 0 | INTERNAL VCO(DEFAULT) |
| 1 | EXTERNAL VCO |

# THEORY OF OPERATION

The ADRF6604 integrates a high performance quadrature down converting mixer with a state of the art fractional-N PLL. The PLL also integrates a low noise VCO. The programmable SPI port allows the user to control the fractional-N PLL functions and the modulator optimization functions as well as allowing for an externally applied LO or VCO.

The quadrature modulator core within the ADRF660x family is the next generation of industry leading family of modulators from Analog Devices. The baseband inputs are converted to currents and then mixed to RF using high-performance NPN transistors. The mixer output currents are transformed to a single-ended RF output using an integrated RF transformer balun. The high performance active mixer core, coupled with the low-loss RF transformer balun results in an exceptional OIP3 and OP1dB, with a very low output noise floor for excellent dynamic range. The use of a passive transformer balun rather than an active output stage leads to an improvement in OIP3 with no sacrifice in noise floor. Over the specified frequency range the four devices in the ADRF660x typically provide RF output P1dB of 15dBm, OIP3 of 30dBm, and RF output noise floor of -157dBm/Hz. Typical image rejection under these conditions is 40dB with no additional I and Q gain compensation. Improved performance at specific frequencies can be achieved with the use of the internal CAPDAC, which is programmable via the SPI port, and through the use of a resistor to VCC at the IP3Set pin (pin 29). Adjustment of the CAPDAC allows increments in phase shift at internal nodes in the 660x, thus allowing cancellation of third order distortion with no change in supply current. Connecting a resistor to VCC from the IP3Set pin increases the internal modulator core current, therefore improving overall IP2 and IP3, as well as P1dB. Using the IP3Set pin for this purpose will increase supply current.

The fractional divide function of the PLL allows the frequency multiplication value from REFIN to LO Out to be a fractional value rather than restricted to an integer as in traditional PLLs. In operation, this multiplication value is INT+(FRAC/MOD) where INT is the integer value, FRAC is the fractional value and MOD is the modulus value, all programmable via the SPI port. In previous frac-N PLL designs, the fractional multiplication was achieved by periodically changing the fractional value in a deterministic way. The down side of this was often spurious components close to the fundamental signal. In the ADRF660x family, a sigma-delta modulator is used to distribute the fractional value randomly, thus significantly reducing the spurious content due to the fractional function.

## PROGRAMMING THE ADRF6604

The ADRF6604 is programmed via a three pin SPI port. The description of timing requirements for the SPI port is given in Figure 2. There are eight programmable registers, each with 24 bits, controlling the operation of the device. The register functions can be broken down as follows;

Register 0 – Integer control for the PLL.

Register 1 – Modulus control for PLL.

Register 2 – Fractional control for PLL.

Register 3 – Sigma Delta Function

Register 4 – PLL Charge pump, PFD, reference path control

Register 5 – LO path and modulator control

Register 6 – VCO controls and VCO enable functions

Register 7 – Modulator bias enable, external VCO enable

Note - The PLL has internal calibration that must be run when the ADRF660x is initialized at a given frequency. This calibration is automatically run whenever registers 0, 1, or 2 are programmed. Because the other registers affect PLL performance, the lower three registers should always be programmed last, preferably in the order 0 – 1- 2.

Software is available on the Analog Devices website (www.analog.com) that allows easy programming from a PC running Windows XP ™.

## LO SELECTION LOGIC

The down converting modulator in the ADRF660x can be used without the internal PLL by applying an external differential LO to pins 37 and 38 (LOP and LON). In addition, when using an LO generated by the internal PLL, the LO signal can be accessed directly at these same pins. This function can be used for debugging purposes or the internally generated LO can be used as the LO for a separate mixer. The operation of the LO generation and whether LOP and LON are input or output is determined by logic levels applied at pin 16 (PLL_EN) and pin 36 (LODRV_EN) as well as bits 3 (LDRV) and 6 (PLEN) in register 5. The combination of externally applied logic and internal bits required for particular LO functions is given in Table 7.

| Pins | | Register Map | | Outputs | |
|---|---|---|---|---|---|
| 16: PLL_EN | 36:LODRV_EN | R5, DB6 PLEN | R5, DB3 LDRV | Output buffer ENB/DSBL | EXT/INT LO |
| 0 | X | 0 | X | DSBL | EXT |
| 0 | X | 1 | X | | |
| 1 | X | 0 | X | | |
| 1 | 0 | 1 | 0 | DSBL | INT |
| 1 | X | 1 | 1 | ENB | INT |
| 1 | 1 | 1 | X | | |

*Table 7. LO Selection Logic*

# OUTLINE DIMENSIONS

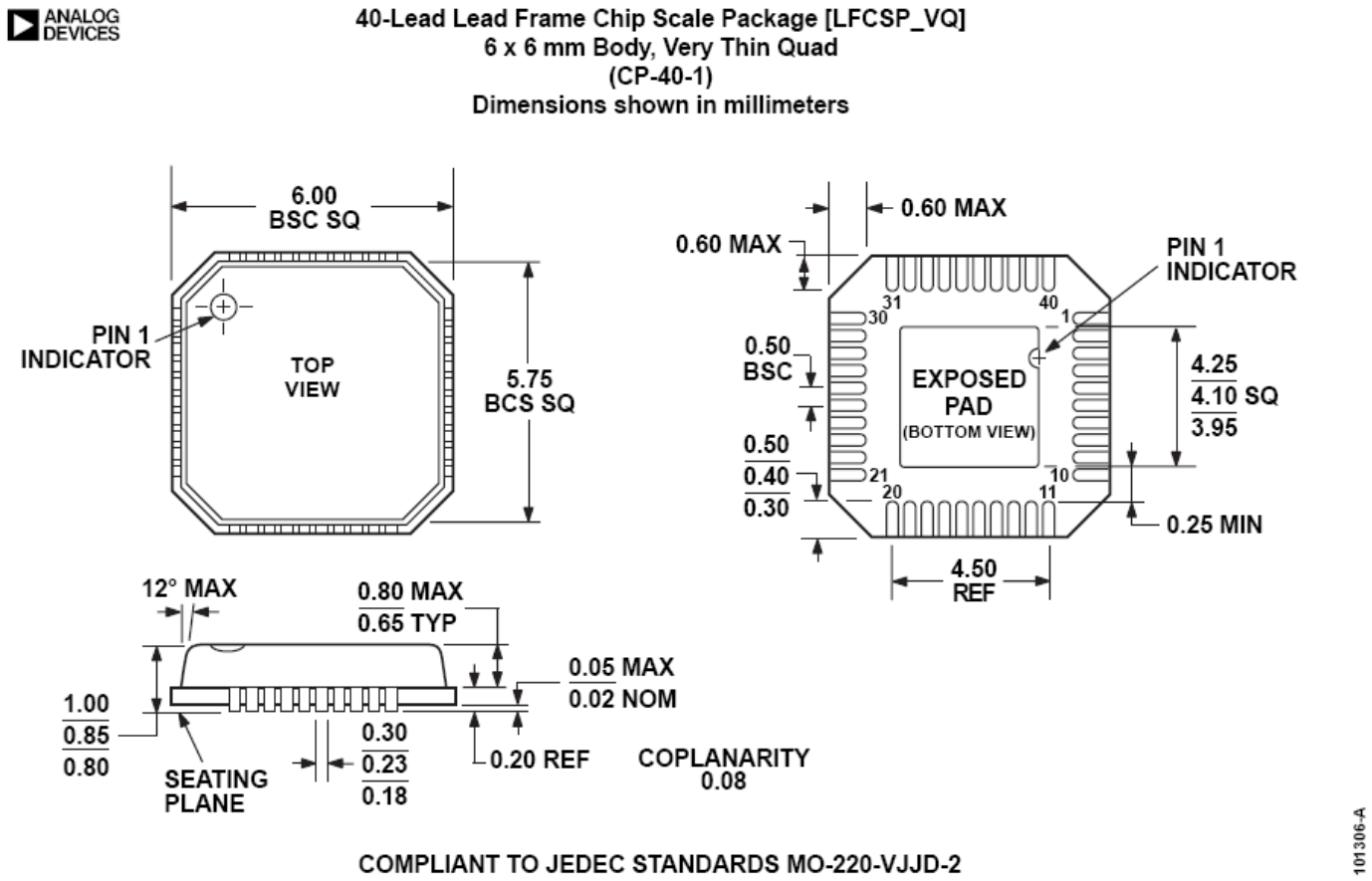


*Figure 4. 40-Lead LFCSP with exposed paddle.*

**TABLE 4. ORDERING GUIDE**

| Model | Temperature Range (°C) | Package Description | Package Option |
|---|---|---|---|
| ADRF6604ACPZ[1] | -40 to +85 | | |

[1] Z indicates Pb-free


PR08553-0-9/09(PrD)